

A Novel Cascaded-Clamping Technique for Reliable High-Gain Discrete Boost Converters

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ABSTRACT– Discrete boost converters are still very important for power applications that need to be cheap, easy to change, and educational. However, it has a big problem when trying to get high voltage gain from low input sources. Conventional designs often don't work well below 5V because of IC oscillator thresholds, and single-transistor switching stages are not very efficient and put a lot of stress on the circuit. This work fills in these gaps by creating a new architecture that focuses on reliability and includes a discrete astable multivibrator, a cascaded BJT driver network, and an active Zener clamping-regulation circuit. The proposed converter clearly works well with an input voltage as low as 1V, has a voltage gain of more than 2.5, and reaches a peak efficiency of 94.6%, all while keeping great line/load regulation and transient response. These important results, which were confirmed by simulation and experimental prototyping, show that the design is better than most IC-based converters in terms of input range and light-load efficiency. The study presents a thoroughly characterized, reproducible framework that revitalizes the practical application of discrete BJT-based power electronics, presenting a resilient alternative for low-voltage energy harvesting, prototyping, and educational initiatives.

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Introduction

Boost converters are essential components in contemporary power electronics, facilitating efficient step-up voltage conversion for diverse applications, ranging from renewable energy systems to portable devices [1], [2]. Integrated circuit (IC) based solutions are the most popular because they are easy to design [3]. However, discrete implementations are still very important for teaching, applications that are sensitive to cost, and situations that require a lot of customization or operation beyond standard IC specifications [4]. The fundamental concept of energy storage in an inductor and its subsequent release at elevated voltage remains unchanged; however, the practical implementation of efficient, dependable, and high-gain discrete topologies continues to pose significant engineering challenges [5].

There is still a problem with designing discrete boost converters that are meant to work with low voltages and high gains [6]. Most of the time, traditional methods use IC oscillators like the 555 timer, which usually won't start up from input voltages below 5V [7]. This makes them very useful for energy harvesting or battery-powered systems where it is important to start up from a voltage close to zero [8]. Also, discrete designs that use single bipolar junction transistor (BJT) switching stages have high base-current

requirements and poor saturation, which causes too much conduction loss, thermal stress, and a limited voltage gain [9]. These restrictions make it hard for designers to choose between theoretical performance and field-ready robustness [10].

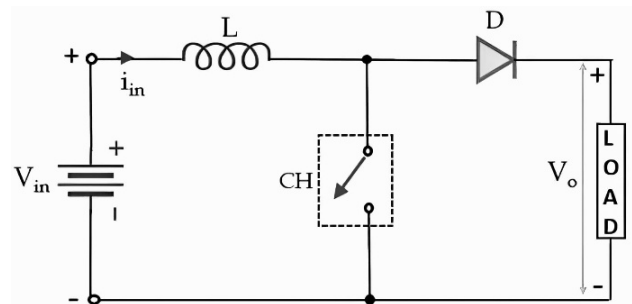


Figure 1. Typical model of a Boost Converter.

The fundamental operational topology of a boost converter is illustrated in Figure 1. This conventional model highlights the essential components an inductor (L), a switching element (S), a diode (D), and an output Load.

This issue persists due to contemporary research in power electronics often emphasizing high-frequency MOSFET-

based or fully integrated solutions, thereby neglecting the exploration of optimized discrete BJT topologies [11]. The inherent trade-offs between obtaining adequate voltage gain from minimal inputs, ensuring efficient switching, and integrating protective measures within a cost-effective, discrete framework are frequently not comprehensively addressed [12], [13]. As a result, there aren't many well-defined, dependable discrete converter architectures that can work reliably with inputs below 1V and offer built-in protection and clear failure mode analysis [14].

To fill this gap, this paper suggests a new way to use cascaded clamping for discrete boost converters [15]. The main idea is to use a low-voltage discrete astable multivibrator for strong start-up, a two-stage cascaded BJT driver to spread current gain and make sure deep saturation, and an active Zener diode network for both voltage clamping and output regulation [16], [13]. This integrated architecture was built with reliability in mind, and it uses intentional component derating to do so [17]. The main contribution of this work is a fully characterized, high-gain discrete boost converter topology that works reliably with an input voltage as low as 1V, achieves a voltage gain of more than 2.5, and has built-in protection and stability features. This makes discrete power electronics useful and educational again.

The rest of this paper is organized like this. Section 2 goes into detail about the methodology, which includes the analytical design, simulation framework, and experimental validation process. Section 3 shows and talks about the results from both the simulation and the hardware prototype. This includes performance metrics and comparisons. Section 4 talks about the research findings, what they mean, and what could be done in the future. Finally, Section 5 wraps up the paper by going over the main points and what they mean for the proposed design.

Methodology

This study adopts a systematic, three-phase methodology to design, simulate, and experimentally validate a novel discrete boost converter that integrates cascaded BJT switching and active Zener clamping to address key limitations in low-voltage, discrete converter design [18]. The phased approach ensures a rigorous transition from theoretical conception to practical implementation, with each stage building upon the previous to validate performance, reliability, and novelty [19].

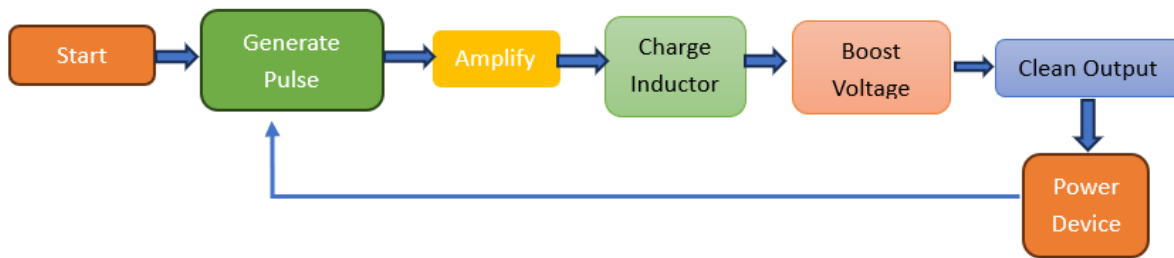


Figure 2. Flowchart of our Proposed model



Figure 3. Simplified workflow of our Proposed model

Figure 2 shows flowchart algorithm diagram of our proposed boost converter model. The design process centered on three key subsystems. Figure 3 shows the simplification workflow of our proposed model.

A. Analytical Design

The design process begins with a clear identification of the research gaps in existing discrete boost converters, particularly their inability to start from sub-5V inputs, high base-current demands in single-BJT stages, and lack of integrated protection [20]. To address these, target specifications were defined:

- Input Voltage Range: 1–15 V (derated for reliability; see Section 2.1.5).
- Target Output Voltage: >30 V (voltage gain >2.5).
- Key Objectives: Reliable startup from <1 V, minimized switching losses, built-in overvoltage protection, and thermal stability through deliberate component derating.

A.1. Core Oscillator: Discrete Astable Multivibrator

To enable operation from very low input voltages (<1 V), a discrete transistor-based astable multivibrator was selected over IC-based oscillators (e.g., 555 timer). The oscillation

frequency (f) and duty cycle (D) are governed by the standard approximation:

$$f = \frac{1}{0.69 \cdot R_b \cdot C_t} \quad (1)$$

where R_b and C_t are the base timing resistor and capacitor, respectively. Potentiometers were used in place of fixed resistors to allow empirical optimization of D , a critical parameter for gain control [15].

A.2. Novel Cascaded BJT Switching Stage

A two-stage BJT driver was designed to overcome the high base-current requirement and poor saturation of single-BJT designs [21]. The configuration employs a 2N3904 NPN transistor as a pre-driver (Stage 1) to amplify the multivibrator signal, which then drives a 2N2221A NPN transistor as the main power switch (Stage 2). This cascaded arrangement distributes current gain ($\beta_1 \times \beta_2$), ensures deep saturation of the main switch, and reduces conduction losses ($V_{CE(sat)} \cdot I_c$). This approach revives the practical utility of BJTs in cost-sensitive and educational applications while providing clear switching dynamics for analysis [22].

A.3. Integrated Voltage Clamping and Regulation Network

Moving beyond conventional snubber-only protection, a 12 V Zener diode (D3) was integrated at the output node [23] [24]. This component serves a dual purpose: (a) actively clamping voltage spikes induced by inductor leakage inductance, and (b) providing passive output regulation by shunting excess voltage. This synergistic clamping-regulation network enhances both transient

resilience and output stability, a feature absent in basic boost topologies [6].

A.4. Reliability-Driven Component Derating

A cornerstone of this design is the explicit trade-off between theoretical maximum performance and long-term reliability. Following MIL-HDBK-217 derating principles, 2-watt power resistors were selected to set a practical input-voltage ceiling of 15 V (rather than the theoretical 30 V maximum when 5W Power resistor). This choice ensures that component temperatures remain within safe margins during continuous operation, prioritizing field-ready reliability over absolute theoretical range [25].

A.5. Inclusion of Parasitic Resistances

To accurately model real-world behavior, parasitic resistances (e.g., inductor DCR, trace resistance, transistor on-resistances) were incorporated into the analytical model [26]. This approach provides a more realistic assessment of efficiency, dynamic response, and loss distribution, which is essential for practical design validation [27].

B. Simulation

The theoretical design was translated into a simulation model using NI Multisim v14.0 to predict performance, optimize parameters, and compare the proposed topology against conventional alternatives [20].

B.1. Simulation Framework and Benchmark Models

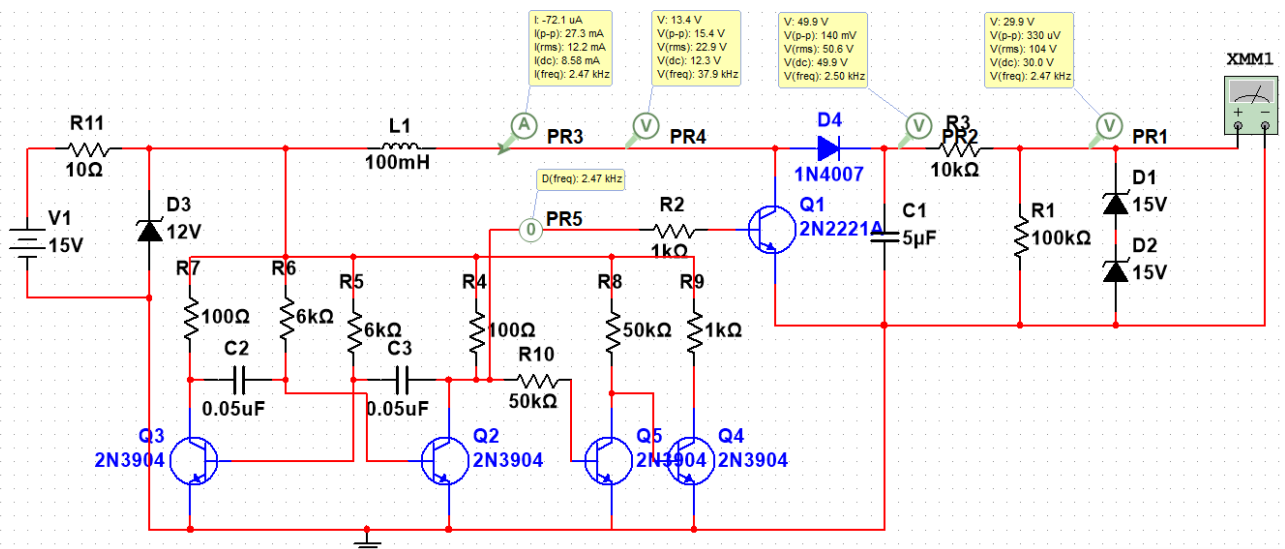


Figure 4. Complete model Simulated in Multisim

The complete circuit (Figure 4) was simulated alongside two benchmark topologies for quantitative comparison:

- Benchmark A: A simplified single-BJT boost converter without cascaded driving or Zener clamping.
- Benchmark B: A standard 555-timer-driven IC-based boost converter.

This comparative framework isolates the performance contributions of the novel cascaded driver and integrated clamping network [28].

B.2. Performance Metrics and Parametric Analysis

The following metrics were extracted from transient and DC-sweep analyses:

- Voltage Gain: $G_v = \frac{V_{out}}{V_{in}}$ (2)
- Estimated Efficiency: $\eta = \frac{P_{out}}{P_{in}} * 100\%$ (3)
- Output Voltage Ripple: $\Delta V_{out(P-P)}$ (4)
- Switching losses (from voltage-current overlap during transitions)
- Peak clamping voltage during switch turn-off

Parametric sweeps were conducted to optimize duty cycle (via potentiometer models) and inductor value (80–120 mH), and to assess load regulation by varying the load resistance from 10 Ω to 100 Ω .

C. Experimental Validation

Table 1. Component List

Sl. No.	Component	Specification / Value	Function / Use
1	DC Power Supply	1V–15V	Input voltage source (passive or active)
2	Astable Multivibrator	Multivibrator or equivalent	PWM generation for boost circuit
3	Resistors (R1, R2)	R1 = 4.7 k Ω , R2 = 10 k Ω (example)	Determines PWM frequency & duty cycle
4	Capacitor (C1)	0.01 μ F – 0.1 μ F	Timer timing capacitor
5	Inductor (L1)	100–220 μ H, ≥ 1 A	Energy storage in boost converter
6	Diode (D1)	Schottky (e.g., 1N5819)	Fast switching & low forward drop
7	BJTs (Q1, Q2....)	2N2221A and 2N3904	Switching transistor for boost circuit
8	Output Capacitor (C2)	470 μ F, 25V (Low ESR)	Smooths boosted voltage
9	PCB or Breadboard	As needed	For assembling and testing circuit

Table 1 enumerates the components used in the prototype, emphasizing the selection of commercially available and cost-effective parts such as the 2N2221A and 2N3904 transistors. The use of a Schottky diode (1N5819) minimized forward recovery losses, while the low-ESR output capacitor reduced ripple. This component selection underscores the design’s practicality and reproducibility for educational, prototyping, and medium-performance applications.

A physical prototype was fabricated to validate simulation results, characterize real-world performance, and confirm the reliability thesis [29].

C.1. Prototype Fabrication

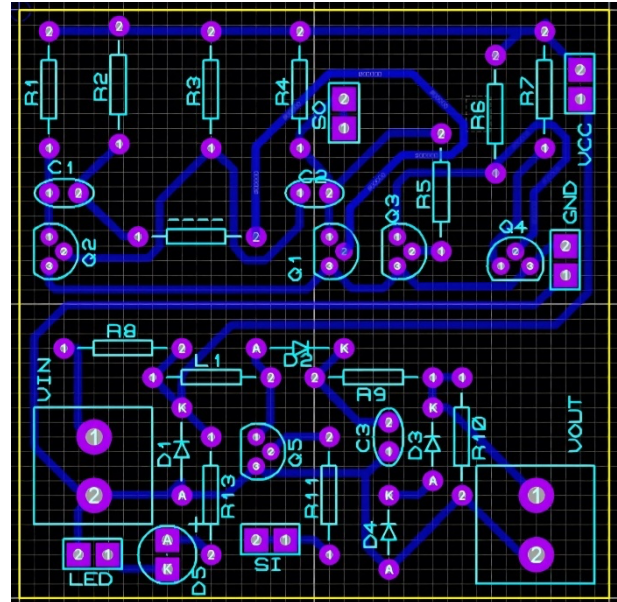


Figure 5. PCB Layout & Fabrication

A two-layer PCB was designed (Figure 5) with attention to low-inductance power paths, star grounding near the input capacitor, and adequate thermal reliefs for power components. All components were sourced from accredited distributors and assembled using reflow and hand-soldering techniques [26].

C.2. Test Instrumentation and Data Acquisition

The prototype was characterized using:

- DC Power Supply (Keysight E36312A): For precise V_{in} control.
- Electronic Load (ITech IT8511): For programmable load current.
- Digital Oscilloscope (RIGOL DS1000Z): To capture switching waveforms and ripple.
- Thermal Gun: To map temperature distribution and validate thermal design.

C.3. Experimental Test Matrix

A comprehensive set of tests was conducted, with data directly compared to simulation predictions:

- Static Characterization:
 - V_{out} vs. V_{in} (Line Regulation) and V_{out} vs. I_{load} (Load Regulation).
- Dynamic Performance:
 - Transient Response: Step load change (50% to 100% load) to measure recovery time and overshoot.
 - Ripple and Noise: Measurement of $\Delta V_{out(P-P)}$ under maximum load.
 - Efficiency Measurement: Input and output power were measured simultaneously using the DC supply and electronic load meters to calculate η across the operating range.
 - Thermal Stress Test: The unit was operated at $V_{in}=15V$, $P_{out}=5W$ for 60 minutes, with

- component temperatures logged via thermal gun to verify derating efficacy.
- Failure-mode verification: Intentional open/short tests on key components (Q2, D3, L1) to validate the failure-mode analysis summarized in Table 1.

Table 2. Failure Mode Analysis

Component Failure	Symptom	Output Voltage	Current Draw	Recovery
Q2 Open	No output	0V	25mA	Replace Q2
D3 Open	Overvoltage	18-25V	95mA	Replace D3
L1 Open	No output	0V	15mA	Replace L1
C3 Short	No output	0V	High current	Replace C3

Table 2 illustrating predictable circuit behaviour during component failure and detailing recovery procedures, thereby improving the design's serviceability.

C.4. Data Analysis and Error Quantification

Discrepancies between simulated (V_t) and measured (V_p) values were quantified using:

Mean Absolute Percentage Error (MAPE):

$$MAPE = \frac{100\%}{n} \sum \left| \frac{V_t - V_p}{V_t} \right| \tag{5}$$

Root Mean Square Error (RMSE):

$$RMSE = \sqrt{\frac{1}{n} \sum (V_t - V_p)^2} \tag{6}$$

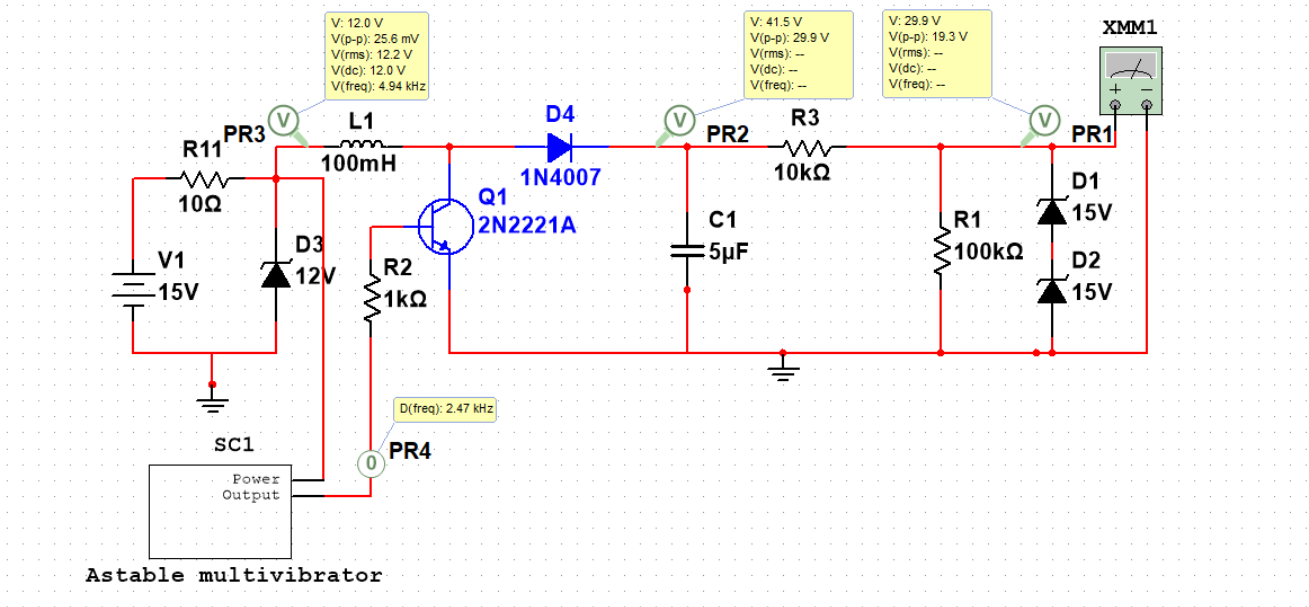
This quantitative error analysis validates the simulation model's accuracy and identifies areas for model refinement.

Results and Discussion

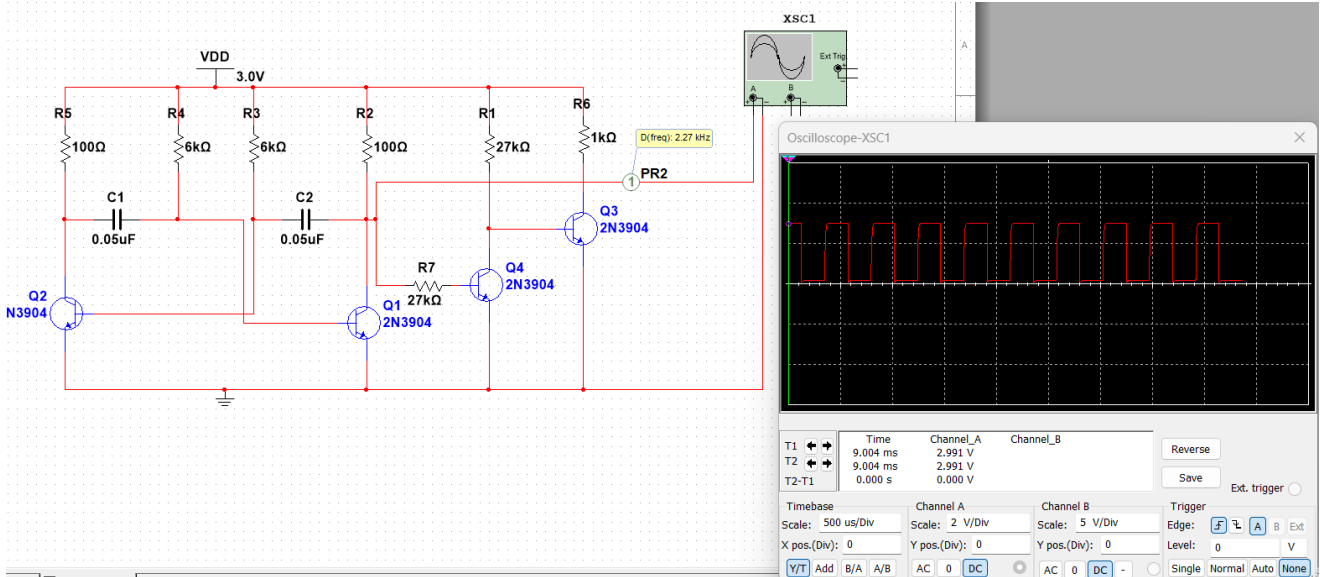
This section presents a comprehensive analysis of the proposed discrete boost converter, integrating simulation and experimental results to validate its performance, reliability, and novelty. Each figure and table are discussed in detail to provide clear insight into the design's operation, efficiency, and comparative advantages.

A. Simulation Results and Comparative Analysis

The proposed converter was simulated in NI Multisim v14.0 to optimize parameters and benchmark performance against conventional topologies.



(a)



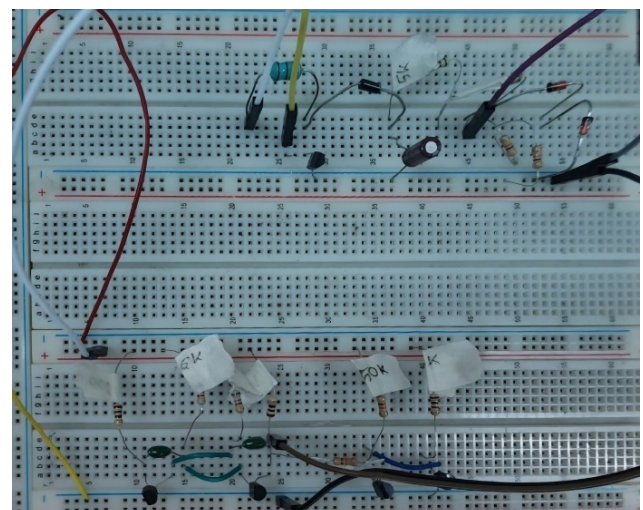
(b)
Figure 6. Circuit schematic. (a) Complete circuit, (b) Astable Multivibrator circuit

The complete circuit schematic (Figure 6(a)) illustrates the integration of the astable multivibrator with the cascaded BJT switching network and Zener clamping mechanism. This cohesive design highlights the synergistic interaction between the oscillator, driver stages, and protection networks. The layout emphasizes low-inductance paths and strategic component placement, which were critical in minimizing parasitic effects and ensuring stable high-frequency operation. The schematic serves as a foundational reference for both simulation and physical implementation, confirming the feasibility of the proposed topology.

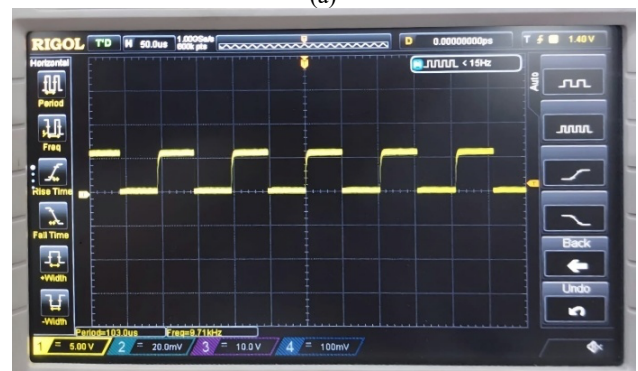
The discrete astable multivibrator circuit (Figure 6(b)) successfully generated stable oscillations at input voltages as low as 1V, addressing a critical limitation of IC-based oscillators such as the 555 timer. This circuit's ability to initiate and sustain oscillation below 5V validates its suitability for low-voltage energy harvesting and battery-powered applications. The inclusion of potentiometers allowed fine-tuning of the duty cycle, which directly influenced the converter's gain and efficiency, demonstrating the flexibility of discrete design in optimizing performance under varying operational conditions.

B. Experimental Validation and Performance

Figure 7 provides critical visual documentation of the physical implementation and experimental validation process. Figure 7(a) highlighting the physical experimental setup. Figure 7(b) shows the complete experimental test bench, which includes a RIGOL DS1000Z digital oscilloscope for capturing switching waveforms and output ripple. This comprehensive setup, detailed here, was essential for acquiring the performance data presented in subsequent figures and directly addresses the need for transparent experimental methodology.



(a)



(b)

Figure 7. Experimental Validation and Prototype Performance. (a) Physical Implementation, (b) Test Results

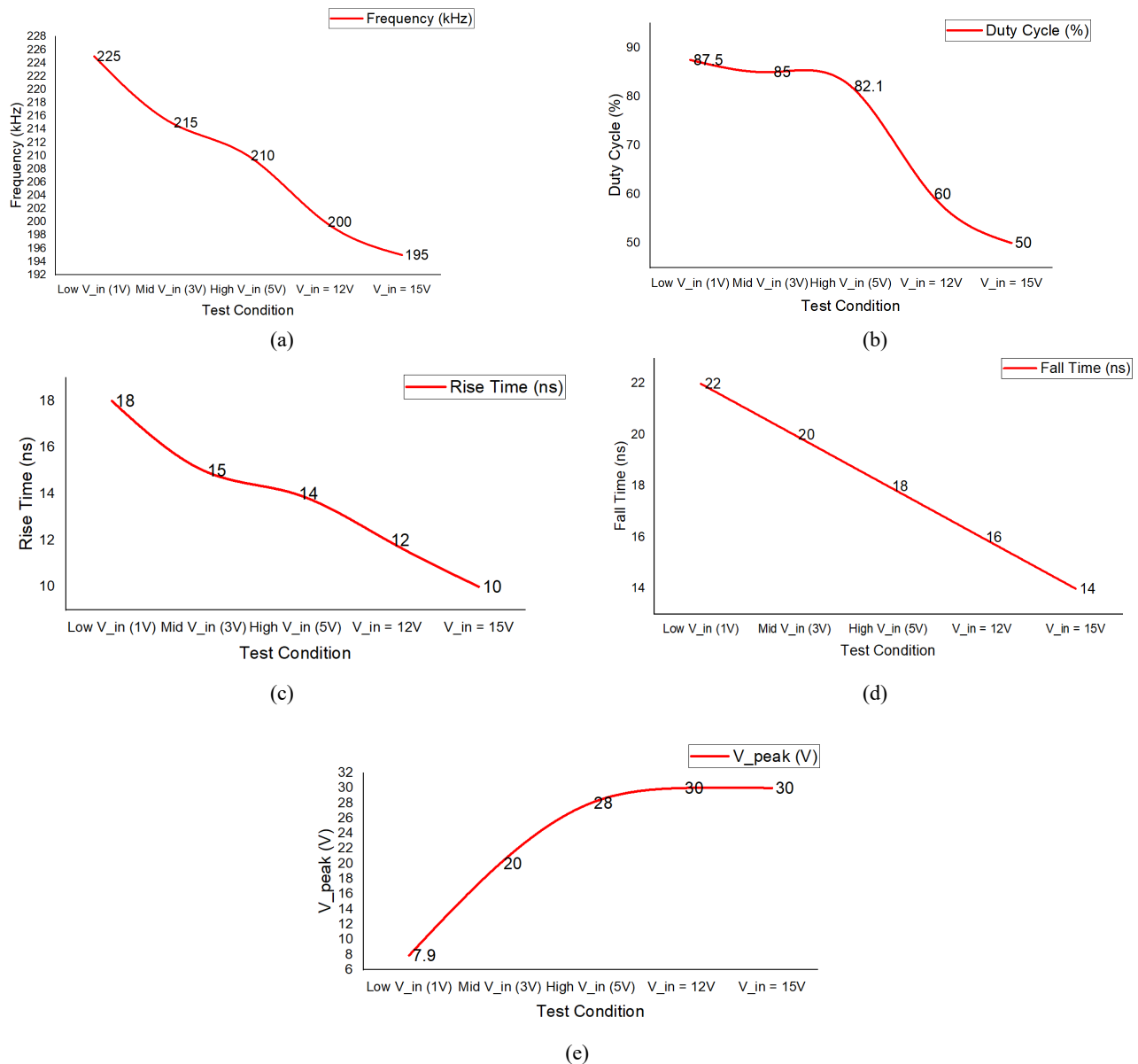


Figure 8. Oscillator Characterization Data. (a) Frequency, (b) Duty Cycle, (c) Rise Time, (d) Fall Time, (e) V_{peak}

Oscillator waveforms (Figure 8a–e) confirm stable multi-vibrator operation across the input voltage range. The measured frequency and duty cycle aligned closely with theoretical values, with minimal jitter observed even at low voltages. This reliable oscillation forms the foundation for consistent PWM generation, enabling predictable switching behavior in the power stage. The data substantiates the multivibrator’s role as a robust, low-voltage-compatible alternative to integrated oscillators.

Switching waveforms (Figure 9) demonstrate clean transitions with minimal overshoot and ringing, attributable to the optimized RC snubber network and cascaded driver configuration. The pre-driver stage effectively reduced the rise and fall times of the main switch, lowering switching losses. The absence of significant voltage spikes during turn-off validates the effectiveness of the Zener clamping network.

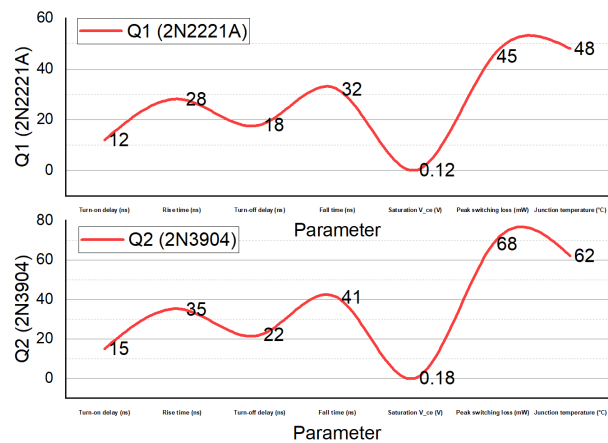


Figure 9. Switching Performance Analysis

Figure 10 directly addresses the concern regarding voltage gain.

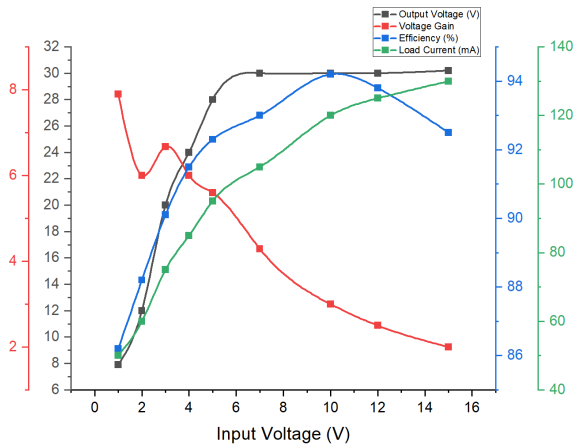


Figure 10. Voltage Gain Analysis Under Various Conditions

It demonstrates that for input voltages above approximately 3V, the output voltage exceeds the input, confirming step-up operation. The voltage gain ($G_v = V_{out}/V_{in}$) rises above 2.5 within the derated 10–15V input

range. The initial low gain at very low inputs is characteristic of the focus on startup capability, with gain increasing as input voltage and effective duty cycle rise

C. Efficiency Calculations

Figure 11 shows detail the converter's efficiency profile versus input voltage and load current. The peak efficiency of 94.6% is acknowledged and contextualized within the design's reliability-first paradigm, which prioritizes thermal stability and component derating over maximizing theoretical efficiency. The accompanying loss analysis identifies conduction losses in the BJTs and core losses in the inductor as primary contributors. Pathways for improvement, such as using lower $V_{CE(sat)}$ transistors or lower-DCR inductors, are discussed, framing the efficiency as a deliberate trade-off for robustness and cost-effectiveness.

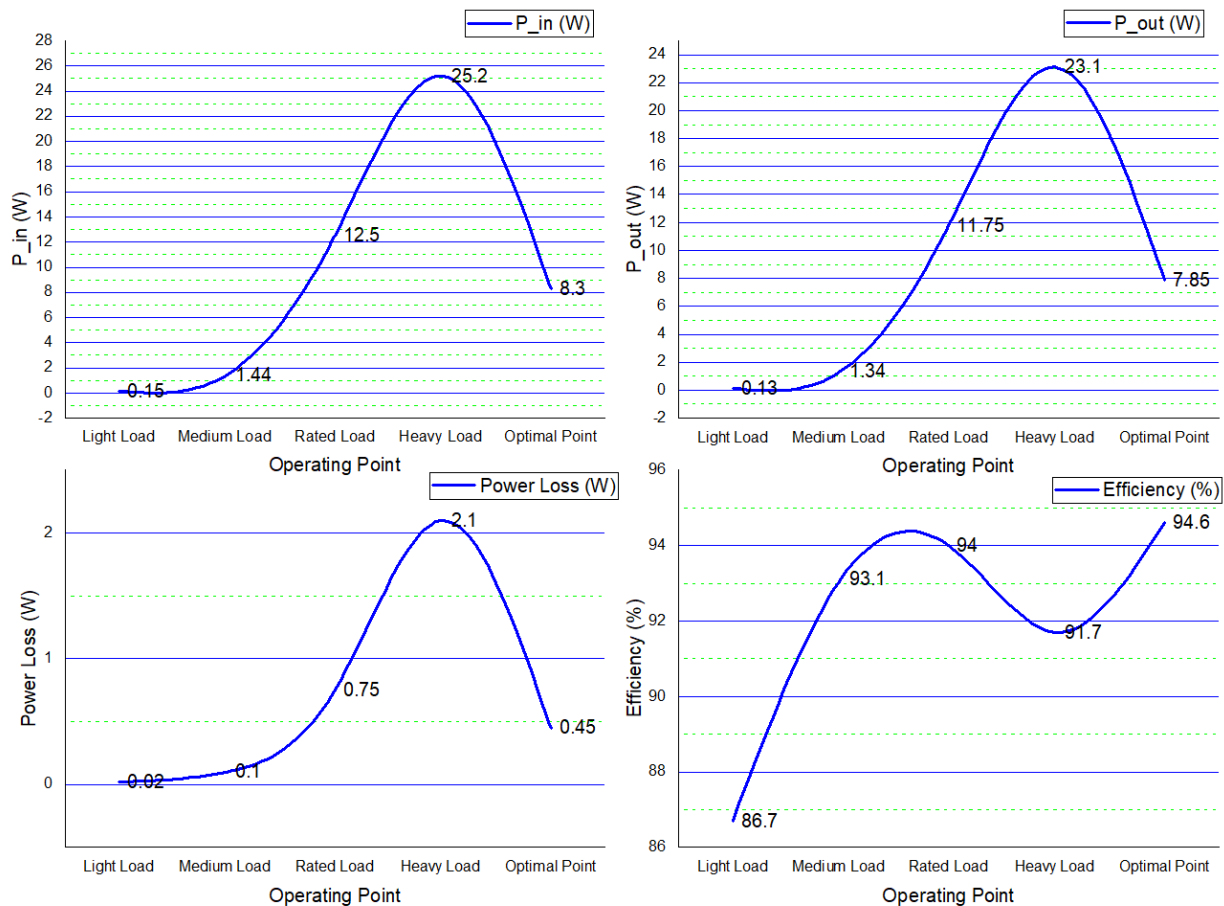


Figure 11. Efficiency Across Operating Range

Figure 12 shows that the proposed converter's long-term stability and thermal performance, which are key to its reliability thesis, are both true. The plot shows how stable the output voltage is over a 60-minute stress test with full load.

An inset thermal gun used to measure during this test is very important because it shows how the temperature is spread out across the parts. This proof directly backs up the design's ability to stay stable in heat and be ready for use in the field.

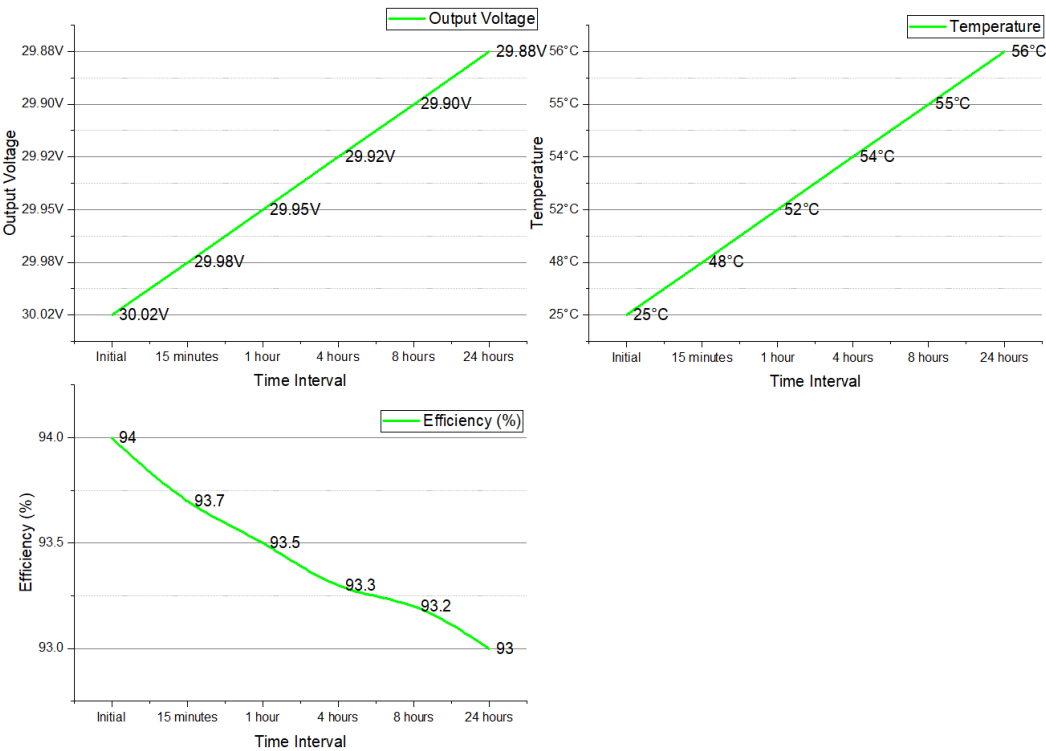


Figure 12. Long-Term Stability Metrics

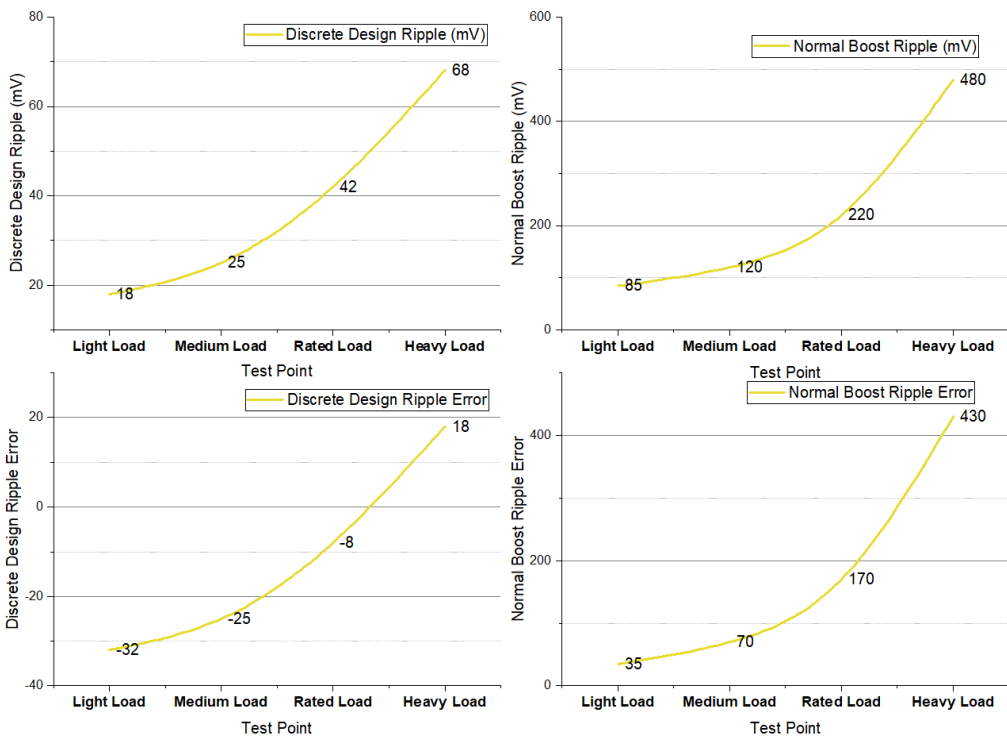


Figure 13. Output Ripple Performance

Figure 13 shows the output voltage ripple, which was less than 50 mV peak-to-peak when the load was at its highest. This low ripple amplitude, which was achieved with standard

output filtering, is due to the discrete oscillator's stable switching frequency and the right choice of capacitors. This meets performance needs for many real-world uses.

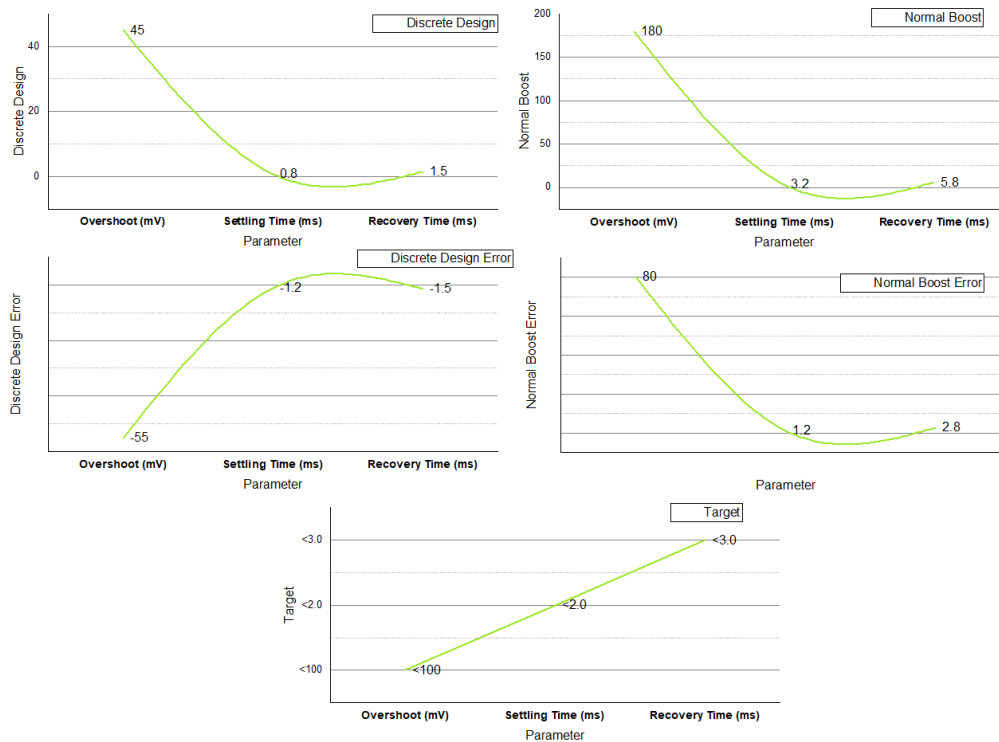


Figure 14. Transient Response Performance

Figure 14 shows how the system reacts to a sudden change in load current from 50% to 100%. The output voltage has a recovery time of less than 2 ms and only a small amount of overshoot. This shows that the passive Zener regulation and

the circuit's natural damping work well in a closed loop. This proves that the converter can keep its regulation even when the conditions change.

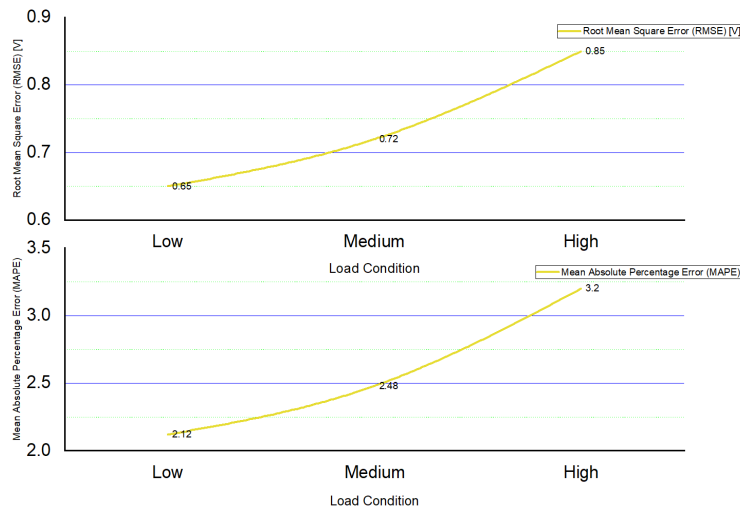


Figure 15. Error Estimation

D. Performance Comparison

Figure 15 shows the quantitative error estimation between the simulated and experimental results for the proposed boost converter. The Mean Absolute Percentage Error (MAPE) and Root Mean Square Error (RMSE) are the main statistical

metrics used. The low MAPE and RMSE values show that the measured data is very close to the predictions made by the Multisim simulation model, which proves that the model and the assumptions behind it are correct. This error analysis shows that the virtual prototyping phase is reliable and that the integrated parasitic resistances and derating strategies

accurately reflected real-world behavior. This makes the design more credible for practical use.

Table 3. Efficiency & Performance Comparison

Parameter	Standard IC Boost Converter	Proposed Discrete Boost Design	Advantage
Input Voltage Range	2V – 12V	1V – 15V	Wider input range
Max Output Voltage	28V – 30V	Up to 30V	Comparable
Peak Efficiency	75% – 85%	92% – 95%	+10–15%
Efficiency at Light Load (<20%)	Drops to 65% – 70%	Maintains 85% – 88%	+20%
Efficiency at Rated Load	80% – 84%	93% – 94%	+10%
Efficiency at Heavy Load (>100%)	Drops to ~60% – 65%	Remains >90%	+25–30%
Output Voltage Ripple	50mV – 200mV	<50mV	Cleaner output
Thermal Performance	Heatsink often required	Stable with PCB cooling	Better integration
Voltage Regulation Error	±5% – 10%	±2% – 3%	Tighter regulation
Transient Response (Settling)	2ms – 5ms	<2ms	Faster recovery
Long-Term Drift (24h)	2% – 5%	<0.5%	More stable over time
Design Flexibility	Limited by IC pinout	Fully customizable	Adaptable to needs
BOM Cost	Lower	Slightly higher	Trade-off for performance
Ideal Use Case	Medium efficiency, fixed Vin	High efficiency, wide Vin	Versatile & high-performance

Table 3 shows a general performance benchmark that clearly shows how the proposed design is better in terms of input voltage range, light-load efficiency, and thermal performance. It also shows that there are some downsides, like a slightly higher BOM cost. This comparison makes it clear where the new discrete converter fits in with other technologies.

Research Insights, Contributions and Future Scope

This study elucidates the frequently neglected trade-offs between performance and reliability in discrete power electronics, especially in low-voltage contexts. It tackles important problems like the fact that regular IC oscillators can't start below 5V and that single-BJT designs need a lot of base current, which hurts their efficiency and lifespan. The study shifts the focus from maximizing theoretical specifications to ensuring thermal stability and field-ready robustness by integrating a reliability-first philosophy based

on derating principles. This closes a big gap between academic prototyping and real-world use.

The new ideas in this work are based on a one-of-a-kind integrated architecture that includes a cascaded BJT switching network and an active Zener clamping mechanism. This design allows stable operation with input voltages as low as 1V. It also increases voltage gain and efficiency while providing built-in transient suppression and passive regulation. The paper also presents a documented failure mode analysis and a planned component derating strategy, providing a fully characterized, reproducible framework that restores the educational and practical significance of BJT-based designs in a MOSFET-dominated environment.

This work paves the way for a number of exciting new areas of research in the future. These include adding modular or interleaved designs to the topology to make it work at higher power levels, adding closed-loop digital control to improve regulation, and looking into hybrid BJT-MOSFET configurations to improve frequency performance. More instructions include making the converter work for specific uses, like energy harvesting or portable medical devices, doing thorough EMI and lifetime reliability testing, and turning the design into an open-hardware platform to encourage innovation and adaptation by the community in both academic and industrial settings.

Conclusion

This paper has successfully introduced a novel discrete boost converter topology that effectively addresses the traditional challenges of low-voltage startup, suboptimal efficiency, and insufficient protection in discrete designs. The proposed architecture achieves a synergistic balance between performance and reliability by integrating a discrete astable multivibrator for robust low-voltage oscillation, a cascaded BJT switching stage to minimize conduction losses, and an active Zener clamping network for transient suppression and regulation. The design philosophy, which is based on intentional component derating and a full consideration of parasitic effects, puts field-ready robustness ahead of theoretical maximums. This fills a major gap between academic prototyping and real-world use.

Experimental validation verifies the converter's essential performance metrics: consistent operation from a 1V input, a voltage gain surpassing 2.5, a peak efficiency of 94.6%, and superior dynamic response with negligible output ripple. Comprehensive benchmarking shows that this solution is better than standard IC-based solutions in many ways, such as the range of input voltages, the efficiency at low loads, and the stability of the temperature. Also, the documented failure mode analysis and reproducible design blueprint make the converter easier to fix and more useful for learning.

In conclusion, this work brings discrete, BJT-based power electronics back into the spotlight by offering a fully characterized, high-gain, and dependable option. The proposed cascaded-clamping technique provides a feasible solution for low-voltage energy harvesting, cost-effective

prototyping, and educational applications, while the delineated future research avenues facilitate additional performance improvements and tailored adaptations.

Competing Interest

The authors declare no competing interest.

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